

Please replace the paragraphs on page 1, starting at line 27 and ending at page 3, line 17 with the following text:

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According to one aspect of the present invention, there is provided a semiconductor device including a first conduction type well region and a second conduction type well region.

The semiconductor device also includes a first gate-gate electrode layer including a gate electrode of a first load transistor and a gate electrode of the first driver transistor and a second gate-gate electrode layer including a gate electrode of a second load transistor and a gate electrode of the second driver transistor. The semiconductor device further includes a first drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of a first driver transistor and a second drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of a second driver transistor. The semiconductor device also includes a first drain-gate wiring layer that forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer and a second drain-gate wiring layer that forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer.

The first load transistor and the second load transistor are provided in the first conduction type well region and first driver transistor and the second driver transistor are provided in the second conduction type well region. The second drain-gate wiring layer is located in a layer over the first drain-gate wiring layer, and has an upper layer of the second drain-gate

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wiring layer and a lower layer of the second drain-gate wiring layer. The upper layer is located in a layer over the lower layer and the upper layer is provided above one of the first conduction type well region and the second conduction type well region.

Please delete the paragraphs starting at page 3, line 18 through page 6, line 20.

Please insert the following paragraphs starting at page 9, line 15.

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According to one aspect of the present invention, there is provided a semiconductor device including a first conduction type well region and a second conduction type well region.

The semiconductor device also includes a first gate-gate electrode layer including a gate electrode of a first load transistor and a gate electrode of the first driver transistor and a second gate-gate electrode layer including a gate electrode of a second load transistor and a gate electrode of the second driver transistor. The semiconductor device further includes a first drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of a first driver transistor and a second drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of a second driver transistor. The semiconductor device also includes a first drain-gate wiring layer that forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer and a second drain-gate wiring layer that forms a part of a connection layer that electrically

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connects the second gate-gate electrode layer and the first drain-drain wiring layer.

The first load transistor and the second load transistor are provided in the first conduction type well region and first driver transistor and the second driver transistor are provided in the second conduction type well region. The second drain-gate wiring layer is located in a layer over the first drain-gate wiring layer, and has an upper layer of the second drain-gate wiring layer and a lower layer of the second drain-gate wiring layer. The upper layer is located in a layer over the lower layer and the upper layer is provided above one of the first conduction type well region and the second conduction type well region.

Here, the "wiring layer" means a conductive layer disposed on a field or an interlayer dielectric layer.

In accordance with the present invention, the second drain-gate wiring layer is located in a layer over the first drain-gate wiring layer. In other words, the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively. As a result, the pattern density of each wiring layer in each of the layers where the first drain-gate wiring layer and the second drain-gate wiring layer are formed, respectively, can be reduced and the cell area can be made smaller, compared to the case where the first drain-gate wiring layer and the second drain-gate wiring layer are formed in the same layer.

In this aspect, as described below, when the upper layer is provided above the second conduction type well region, a main word line can be readily provided above the first conduction type well region. Also, when the upper

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layer is provided above the first conduction type well region, a main word line can be readily provided above the second conduction type well region.

Accordingly, the semiconductor device of this aspect may have one of the following arrangements:

(1) The upper layer may be provided above the second conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

With this arrangement, the main word line may be provided in the same layer as the upper layer, and may be provided above the first conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

(2) The upper layer may be provided above the first conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

With this arrangement, the main word line may be provided in the same layer as the upper layer, and may be provided above the second conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

Further, the semiconductor device in accordance with this aspect may include one of the following arrangements:

(3) The first drain-gate wiring layer may be electrically connected to the second drain-drain wiring layer through a contact section, the lower layer may be electrically connected to the second gate-gate electrode layer through a contact section, and the upper layer may be electrically connected to the

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first drain-drain wiring layer and the lower layer through contact sections, respectively.

(4) The first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer may be provided in the same layer, and the first drain-gate wiring layer may be provided over a border between the first conduction type well region and the second conduction type well region.

(5) The first drain-gate wiring layer and the upper layer may be provided in a manner not to overlap one another as viewed from a vertical direction.

(6) The first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer may be located in a first conductive layer, the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer may be located in a second conductive layer, and the upper layer may be located in a third conductive layer.

(7) A second conductive layer may be a nitride layer of a refractory metal (for example, titanium nitride). As a result of the second conductive layer being a nitride layer of a refractory metal, the thickness of the second conductive layer can be reduced, and miniature processing can be readily performed. Accordingly, the cell area can be reduced.

(8) A second conductive layer may have a thickness of 100 to 200nm.

2. Memory System

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A memory system in accordance with another aspect of the present invention is provided with the above described semiconductor device.

3. Electronic Apparatus

An electronic apparatus in accordance with further aspect of the present invention is provided with the above described semiconductor device.

IN THE ABSTRACT:

Please replace the original Abstract of the Disclosure with the attached Abstract of the Disclosure.

IN THE CLAIMS:

Please replace the text of claims 1, 12 and 13 with the following text.

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1. A semiconductor device comprising:
 - a first conduction type well region;
 - a second conduction type well region;
 - a first gate-gate electrode layer including a gate electrode of a first load transistor and a gate electrode of a first driver transistor;
 - a second gate-gate electrode layer including a gate electrode of a second load transistor and a gate electrode of a second driver transistor;
 - a first drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor;

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a second drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor;

a first drain-gate wiring layer that forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer; and

a second drain-gate wiring layer that forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer,

wherein the first load transistor and the second load transistor are provided in the first conduction type well region,

wherein the first driver transistor and the second driver transistor are provided in the second conduction type well region,

wherein the second drain-gate wiring layer is located in a layer over the first drain-gate wiring layer, and has an upper layer of the second drain-gate wiring layer and a lower layer of the second drain-gate wiring layer,

wherein the upper layer is located in a layer over the lower layer, and

wherein the upper layer is provided above one of the first conduction type well region and the second conduction type well region.

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12. A memory system provided with the semiconductor device according to claim 1.

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13. An electronic apparatus provided with the semiconductor device according to claim 1.

Please add the following new claims:

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14. (Newly Added) A semiconductor device comprising:
a first conduction type well region;
a second conduction type well region;
a first gate-gate electrode layer including a gate electrode of a first load transistor and a gate electrode of a first driver transistor;
a second gate-gate electrode layer including a gate electrode of a second load transistor and a gate electrode of a second driver transistor;
means for electrically connecting a drain region of the first load transistor and a drain region of the first driver transistor;
means for electrically connecting a drain region of the second load transistor and a drain region of the second driver transistor;
means for electrically connecting the first gate-gate electrode layer and a second drain-drain wiring layer; and
means for electrically connecting the second gate-gate electrode layer and a first drain-drain wiring layer,
wherein the first load transistor and the second load transistor are provided in the first conduction type well region,
wherein the first driver transistor and the second driver transistor are provided in the second conduction type well region,

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wherein a second drain-gate wiring layer is located in a layer over a first drain-gate wiring layer, and has an upper layer of the second drain-gate wiring layer and a lower layer of the second drain-gate wiring layer,

wherein the upper layer is located in a layer over the lower layer, and

wherein the upper layer is provided above one of the first conduction type well region and the second conduction type well region.

15. (Newly Added) The semiconductor device according to claim 14, wherein the upper layer is provided above the second conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

16. (Newly Added) The semiconductor device according to claim 15, further comprising a main word line, wherein the main word line is provided in the same layer as the upper layer, and is provided above the first conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

17. (Newly Added) The semiconductor device according to claim 14, wherein the upper layer is provided above the first conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

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18. (Newly Added) The semiconductor device according to claim 17 further comprising a main word line, wherein the main word line is provided in the same layer as the upper layer, and is provided above the second conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

19. (Newly Added) The semiconductor device according to claim 14, wherein the first drain-gate wiring layer is electrically connected to the second drain-drain wiring layer through a contact section, wherein the lower layer is electrically connected to the second gate-gate electrode layer through a contact section, and wherein the upper layer is electrically connected to the first drain-drain wiring layer and the lower layer through contact sections, respectively.

20. (Newly Added) The semiconductor device according to claim 14, wherein the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer are provided in the same layer, and wherein the first drain-gate wiring layer is provided over a border between the first conduction type well region and the second conduction type well region.

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21. (Newly Added) The semiconductor device according to claim 14, wherein the first drain-gate wiring layer and the upper layer are provided in a manner not to overlap one another as viewed from a vertical direction.

22. (Newly Added) The semiconductor device according to claim 14, wherein the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer are located in a first conductive layer,

wherein the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer are located in a second conductive layer, and

wherein the upper layer is located in a third conductive layer.

23. (Newly Added) The semiconductor device according to claim 14, wherein a second conductive layer is a nitride layer of a refractory metal.

24. (Newly Added) The semiconductor device according to claim 14, wherein a second conductive layer has a thickness of 100 to 200nm.
